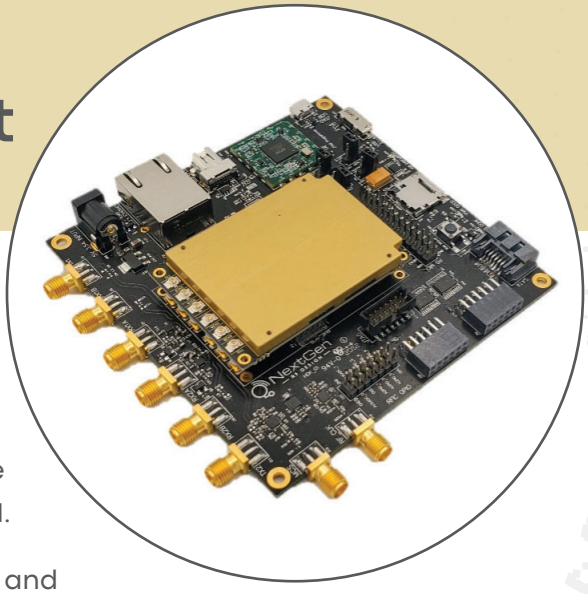
BytePipe x9002
Hardware Development Kit



The BytePipe SDR Development Kit consists of a Hardware Development Kit (HDK) main board combined with a Software Defined Radio (SDR) System on a Module (SOM) and supporting cables, power supply and software to enable testing and development with the NextGen RF BytePipe SOM.

The SOM Development Kit can be used as an evaluation tool and prototyping platform to aid in integration of the SOM into a full-scale product, or as a starting point to explore custom development of an SDR transceiver.

HIGHLIGHTS

FEATURES

- USB 2.0/3.0 Host/Device/OTG Connector
- 10/100/1000 Ethernet Connector
- Display Port Connector
- SATA Interface Connector
- JTAG/UART Interface
- RF Device Clock & MCS
- SD Card Slot
- AC Power Supply and Power Regulators
- SOM Heatsink and Fan
- Square Form Factor - 4.25" x 4.25" (PCB Only)

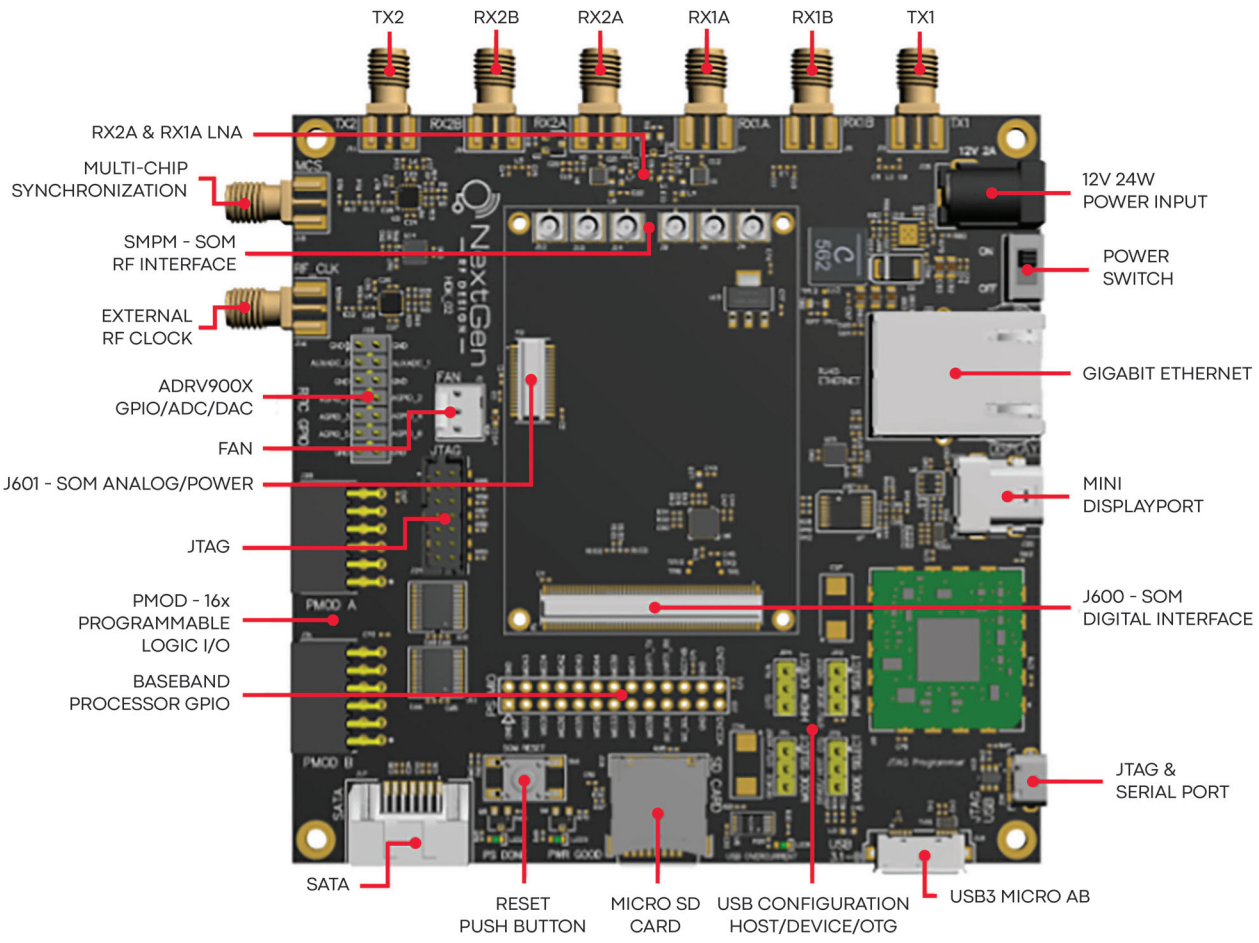
PACKAGE CONTENTS

- Developer Kit Main Board
- BytePipe SDR SOM module (PN: BP_3CG1E_9002)
- 6 - SOM RF Interconnects
- SOM Heatsink & Fan
- Power Supply
- USB & Ethernet Cables
- SD Card with link to startup guide and pre-installed software
- 6 Hours NextGen RF Engineering Support

A PRODUCT OF

NextGen
RF DESIGN

Hardware Overview



Theory of Operation

The SOM requires a carrier board to supply power and provide access to its peripherals. NextGen RF Design provides this hardware development kit (HDK) described in following sections.

Power

The power jack supplies power to the HDK and SOM.
A nominal 12V 24W power supply should be connected using a 2.1 mm x 5.5 mm barrel jack. Although 12V is suggested, the input can range from 7V to 24V as long as the supply is capable of sourcing 24W.

Power Switch

The power switch is next to the power jack and clearly labeled "on" and "off". When turned on a 5.0V regulator supplies power to the HDK, SOM and fan.

Ethernet

The Ethernet signals are accessible through J600.

Display Port

Signal	J600 Pin	Description
DP_OE	MIO29	AUX Channel Output Enable
DP_AUX_OUT	MIO27	AUX Channel Output
DP_AUX_IN	MIO30	AUX Channel Input
DP_HPD	MIO28	Data Pairs
DP_LANE0_P	GTR_TX[2]_P	Hot-Plug Detect
DP_LANE0_N	GTR_TX[2]_N	Data Pairs
DP_LANE1_P	GTR_TX[3]_P	Data Pairs
DP_LANE1_N	GTR_TX[3]_N	Data Pairs

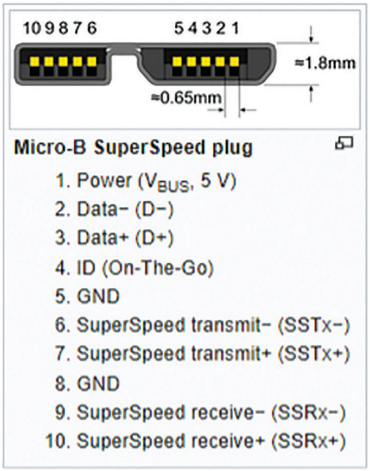
The HDK uses the MIO pins combined with dual GTR channels to support a 4K DisplayPort output.

Hardware Overview

USB

Jumper	Host Mode	Device Mode	OTG Mode
JP1	1-2	Open	1-2
JP2	1-2	2-3	2-3
JP3	2-3	2-3	1-2
JP4	1-2	2-3	2-3

The HDK supports USB2 and USB3.0 by combining the USB signals from the SOM with a single GTR land. A micro-B USB connector allows for USB2 or USB3.0 along with Device, Host or OTG modes. The table above shows the jumper locations for configuring the appropriate modes.



SD Card

Signal	J600 Pin	Description
SD1_DATA0	MIO46	Data
SD1_DATA1	MIO47	Data
SD1_DATA2	MIO48	Data
SD1_DATA3	MIO49	Data
SD1_CMD	MIO50	Command
D1_CLK	MIO51	Clock
SD1_DETECT	MIO45	Detect

The HDK implements an SD card using the above MIO signals.

SATA

The HDK implements a 6Gbps SATA interface using GTR_TX1 and GTR_RX1 signals.

PS MIO

Description	Signal	Pin	Pin	Signal	Description
Ground	GND	1	2	GND	Ground
GPIO	MIO32	3	4	MIO43	GPIO
GPIO	MIO31	5	6	MIO34	GPIO
GPIO	MIO36	7	8	MIO42	GPIO
GPIO	MIO35	9	10	MIO40	GPIO
GPIO	MIO26	11	12	MIO44	GPIO
GPIO	MIO33	13	14	MIO39	GPIO
GPIO	MIO37	15	16	MIO41	GPIO
GPIO	MIO38	17	18	UART1_RX	UART1 Rx Input
12C Clock	12C1_SCL	19	20	UART1_TX	UART1 Tx Output
12C Data	12C1_SDA	21	22	VCC1V8	1.8V VCC
Ground	GND	23	24	GND	Ground
3.3V VCCIO	VCC3V3	25	26	VCC3V3	3.3V VCCIO

The HDK routes unused MIO signals to J23.

RFIC MIO

Description	Signal	Pin	Pin	Signal	Description
Ground	GND	1	2	GND	Ground
ADC Input	AUXADC_0	3	4	AUXADC_1	GPIO
Ground	GND	5	6	GND	Ground
GPIO or DAC	AGPIO_1	7	8	AGPIO_2	GPIO or DAC
GPIO or DAC	AGPIO_3	9	10	AGPIO_4	GPIO
GPIO	AGPIO_5	11	12	AGPIO_6	GPIO
Ground	GND	13	14	GND	Ground

The HDK routes unused RFIC GPIO to J22.

RF Clock

The HDK allows for an external RF clock to be connected to J16. Software can be configured to enable this clock.

MCS

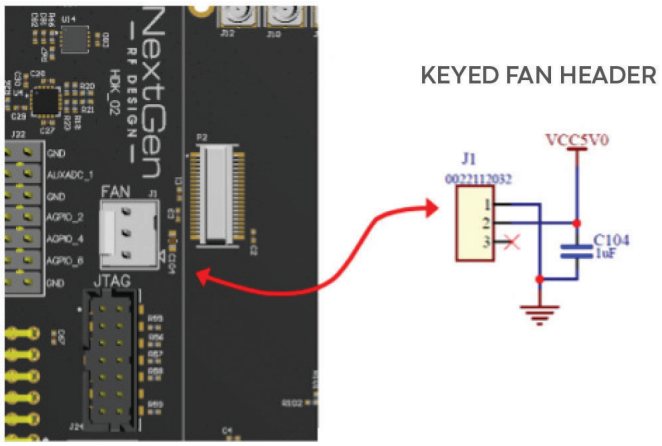
The HDK allows for an external MCS signal to be connected to J15. Software can be configured to enable this functionality.

Hardware Overview

Fan

Signal	J1 Pin	Description
VCC5V0	1	Fan Supply
GND	2	Ground
	NC	No Connect

The HDK supports a 3pin 5V Fan connection using J1.



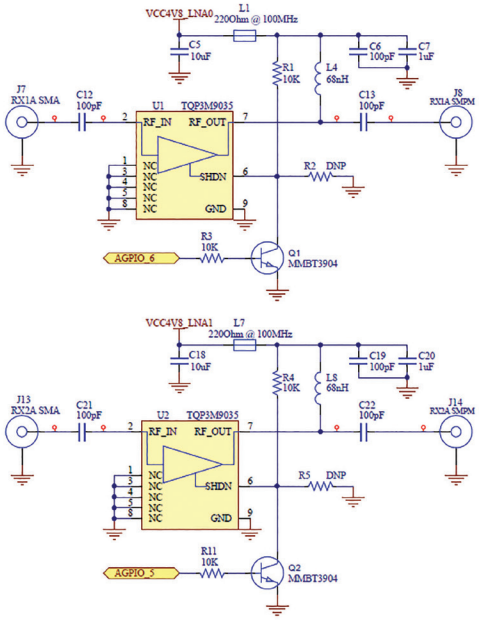
RF SMA Ports

Signal	Connector	Description
TX1	J3	Transmit Channel 1 Direct Connection
TX2	J11	Transmit Channel 2 Direct Connection
RX1A	J7	Receive Channel 1 with LNA
RX2A	J13	Receive Channel 2 with LNA
RX1B	J5	Receive Channel 1 Direct Connection
RX2B	J9	Receive Channel 2 Direct Connection

The HDK provides direct access to the SOM transmit and receive RF ports. In addition, each receiver can be routed through a TQP3M9035, 50 - 6000 MHz High Linearity Low Noise Amplifier Gain Block on the HDK.

LNA

LNA Enable Pin	Receive Port	Connector	Description
AGPIO_6	RX1A	J22.12	Add jumper between enable pin and 1.8V
AGPIO_5	RX2A	J22.11	Add jumper between enable pin and 1.8V



PMOD

PMODA - J28

SOM Signal	HDK Signal	Pin	Pin	HDK Signal	SOM Signal
IO_L1_P	PMOD_A0_P	1	7	PMOD_A2_P	IO_L3_P
IO_L1_N	PMOD_A0_N	2	8	PMOD_A2_N	IO_L3_N
IO_L2_P	PMOD_A1_P	3	9	PMOD_A3_P	IO_L4_P
IO_L2_N	PMOD_A1_N	4	10	PMOD_A3_N	IO_L4_N
Ground	GND	5	11	GND	Ground
3.3V	VCC3V3	6	12	VCC3V3	3.3V

PMODB - J31

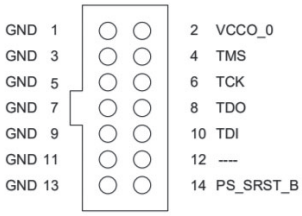
SOM Signal	HDK Signal	Pin	Pin	HDK Signal	SOM Signal
IO_L5_P	PMOD_B0_P	1	7	PMOD_B2_P	IO_L11_P
IO_L5_N	PMOD_B0_N	2	8	PMOD_B2_N	IO_L11_N
IO_L10_P	PMOD_B1_P	3	9	PMOD_B3_P	IO_L12_P
IO_L10_N	PMOD_B1_N	4	10	PMOD_B3_N	IO_L12_N
Ground	GND	5	11	GND	Ground
3.3V	VCC3V3	6	12	VCC3V3	3.3V

The HDK routes the baseband processor programmable logic I/O through two PMODs, J28 and J31. All signals are level shifted from 1.8V to 3.3V to comply with the PMOD standard.

Hardware Overview

JTAG

The HDK supports access to the JTAG signals through an on board Digilent USB programming module or through a standard 14-pin Xilinx System Board Header. Either connection can be used without hardware configuration.



Serial Port

The HDK provides serial port access through the UART0 signals via the Digilent programming module. An additional serial port connection can be made using the UART1 signals on J23.

Reset Button

The HDK connects PS_SRST_N to SW1 providing a push button reset to the user.