

DATE	REQUESTER	DESCRIPTION OF THE CHANGE	EDITOR
04/17/2020	Elliott Nelson	Created	Elliott Nelson
12/15/2020	Elliott Nelson	Revision 1	Elliott Nelson
6/15/2021	Elliott Nelson	Revision 2	Elliott Nelson
6/15/2021	Elliott Nelson	Add Test Points to U6.8, U6.9, U6.11, U6.12, U6.13, U6.14, U6.16, U6.17, U6.19, U6.20	Mike Larsen
6/15/2021	Elliott Nelson	Change R63 to pull up to VCC3V3 instead of VCC1V8	Mike Larsen
6/15/2021	Elliott Nelson	Add TPS54561 and supporting circuits.	Mike Larsen
6/15/2021	Elliott Nelson	Add Fan connector to the 5V supply.	Mike Larsen
6/15/2021	Elliott Nelson	Add A Slide switch for main power control.	Mike Larsen
6/15/2021	Elliott Nelson	Swap I2C1_SCL and I2C1_SDA on P1	Mike Larsen



uSD Card
NewEgg
9SIA12K9731719
16GB



SOM Screw
McMASTER-CARR
92000A007
M1.6x0.35mm x 12mm



SOM Screw
McMASTER-CARR
92000A007
M1.6x0.35mm x 12mm



SOM Screw
McMASTER-CARR
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M1.6x0.35mm x 12mm



SOM Screw
McMASTER-CARR
92000A007
M1.6x0.35mm x 12mm



Spacer



Spacer



Spacer



Spacer



Nut



Nut




Nut



Nut

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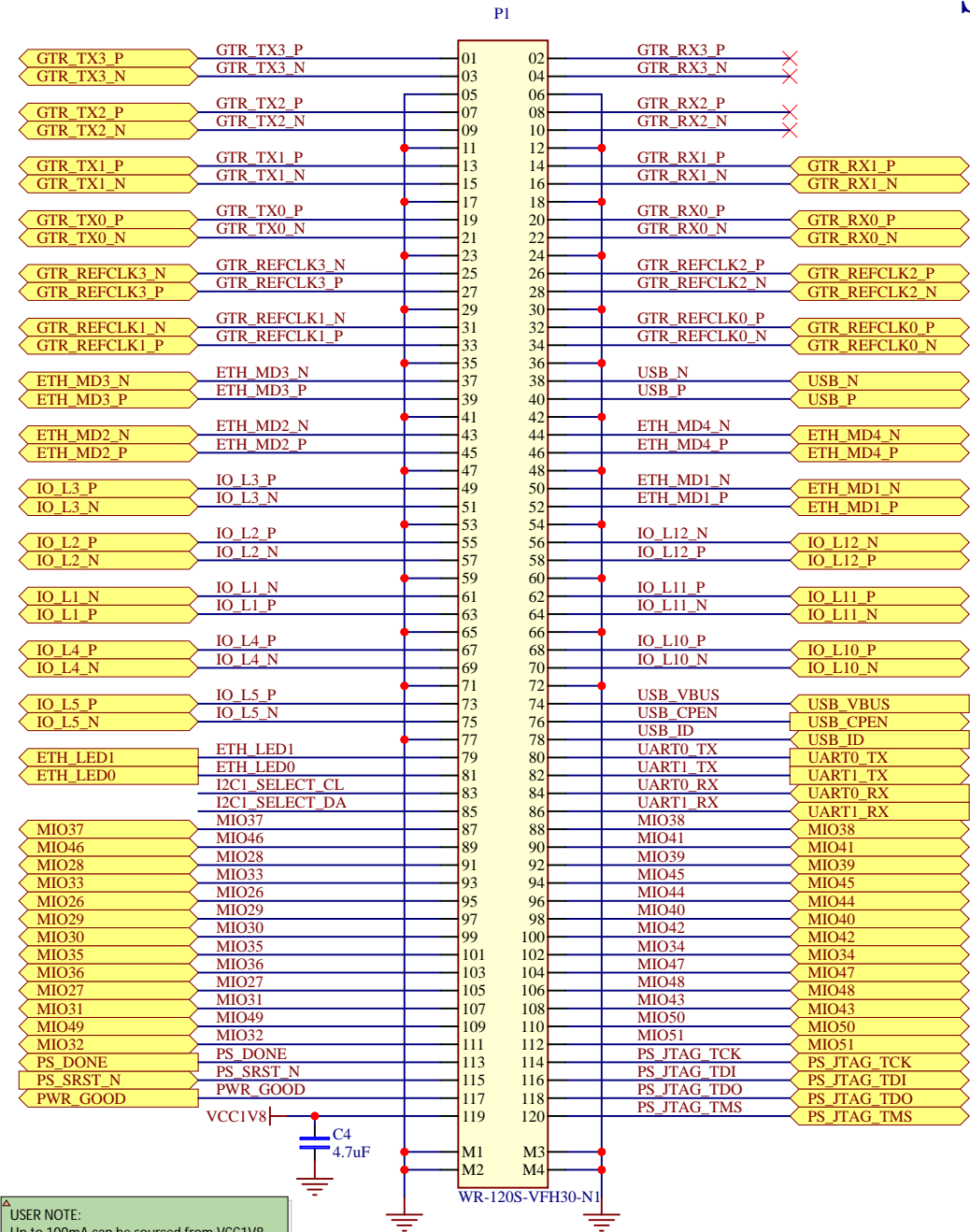
ENGINEER:	ELLIOTT NELSON
SYSTEM ENGINEER:	LUKE THOLEN
DATE:	10/11/2021



NextGen RF Design
2130 Howard Dr W
North Mankato, MN 56003

CUSTOMER: NextGen RF Design	
PROJECT: BytePipe X9002_HDK	
PAGE TITLE: Notes	
SIZE B	VARIANT: [No Variations]
SHEET 1 OF 7	
REV: 2	

SOM INTERCONNECT

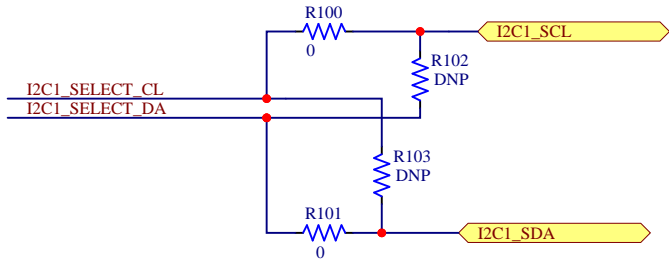
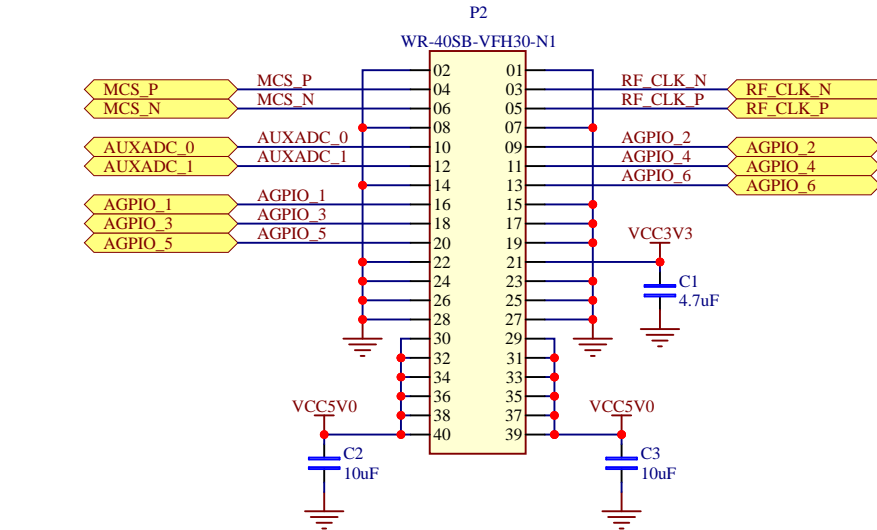


USER NOTE:
Up to 100mA can be sourced from VCC1V8.

PS_DONE, PS_SRST_N, PWR_GOOD, and JTAG reference VCC1V8 supply.

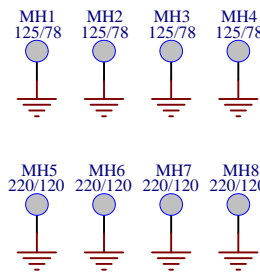
USER NOTE:

- Four GTR transceiver channels are shared with five high-speed serial I/O peripherals including PCIe, SATA, DisplayPort, USB3.0, and GMII. These are powered from a 1.8V.
- UART0, UART1, and I2C1 peripherals are powered from VCC0_PSIQ_501 provided from the host.
- Multiplexed IO 26-51 are powered from VCC0_PSIQ_501 provided by the host. These pins can be multiplexed across a variety of peripheral s or be used as GPIO. When combining the display port IO with GTR channels up to 4k 60fps video can be supported.
- PL IO supports differential or single ended IO. These IO are powered at 1.8V and connect to BANK 65. Some of these pins also support connection to the ADC.
- USB OTG signals support USB2.0 host or device. They can be combined with GTR channels to support USB 3.0.



USER NOTE:
I2C Selection Resistors.

Rev 1 BytePipe populate 0 Ohm resistors R100 & R101. Future Designs populate 0 Ohm resistors R102 & R103.




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NextGen RF Design
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North Mankato, MN 56003

CUSTOMER: NextGen RF Design

PROJECT: BytePipe X9002_HDK

PAGE TITLE: SOM Interface

SIZE	VARIANT:	SHEET	REV:
B	[No Variations]	2 OF 7	2

USER NOTE:
Compatible Host Connectors. Note 7mm connector required for use with SMPM adapters.

Stackup	J1	J2
4mm	WR-120SB-VF-N1	WR-40SB-VF-N1
4mm	WR-120S-VF-N1	WR-40S-VF-N1
7mm	WR-120SB-VFH30-N1	WR-40SB-VFH30-N1
7mm	WR-120S-VFH30-N1	WR-40S-VFH30-N1

DESIGN NOTE:
The power and digital signals are routed over separate connectors to minimize noise, pin count, and to optimize PCB routing.

Power connector supports 0.3A per pin.

VCC5V0: 5.0V @ 2.75A max

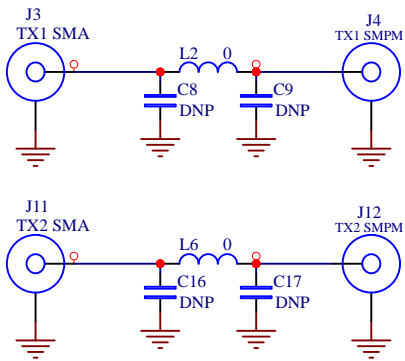
USER NOTE:
Analog GPIO operate at 1.8V nominally.

AGPIO[3:0] each supports GPIO or can be individually configured as an auxiliary DAC output. The DACs are 12bits and have a output voltage range from 0.05V to VDDA_1P8-0.05V with a current drive of 10mA.

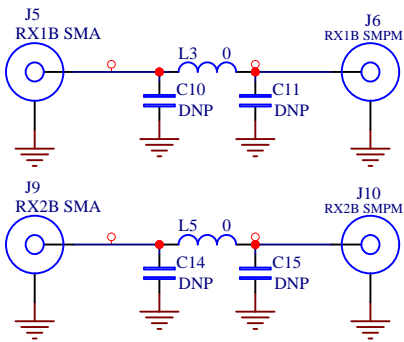
The AUX ADC is 10 bits with input voltage range of 0.05V to 0.95V.

The Multi-chip Synchronization (MCS) signal allows for multiple ADRV9002 devices to be synchronized. When MCS is used a common RF_CLK must be shared across devices.

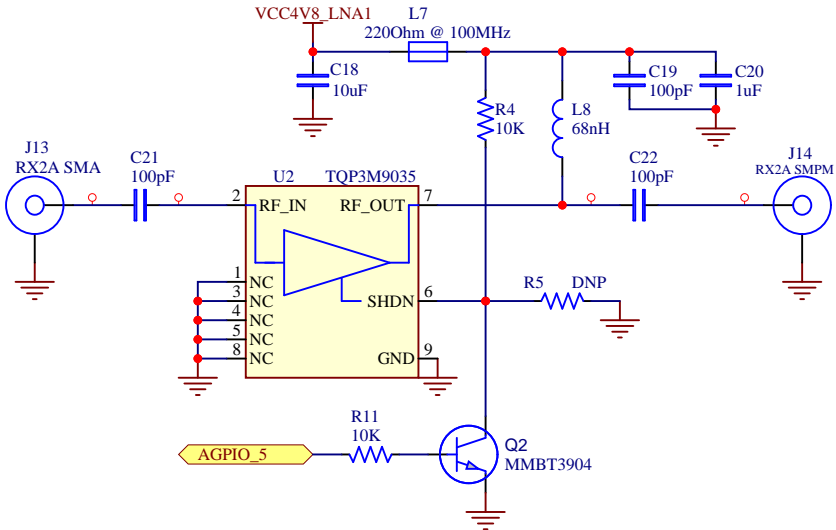
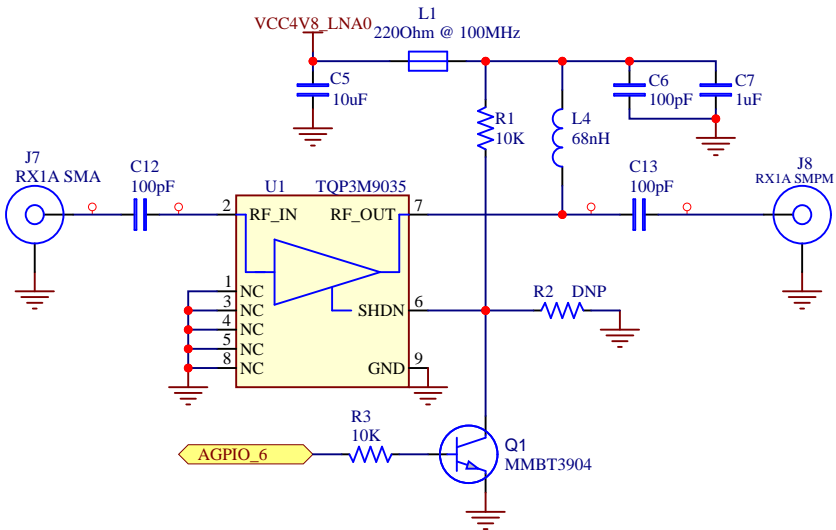
TRANSMIT PORTS



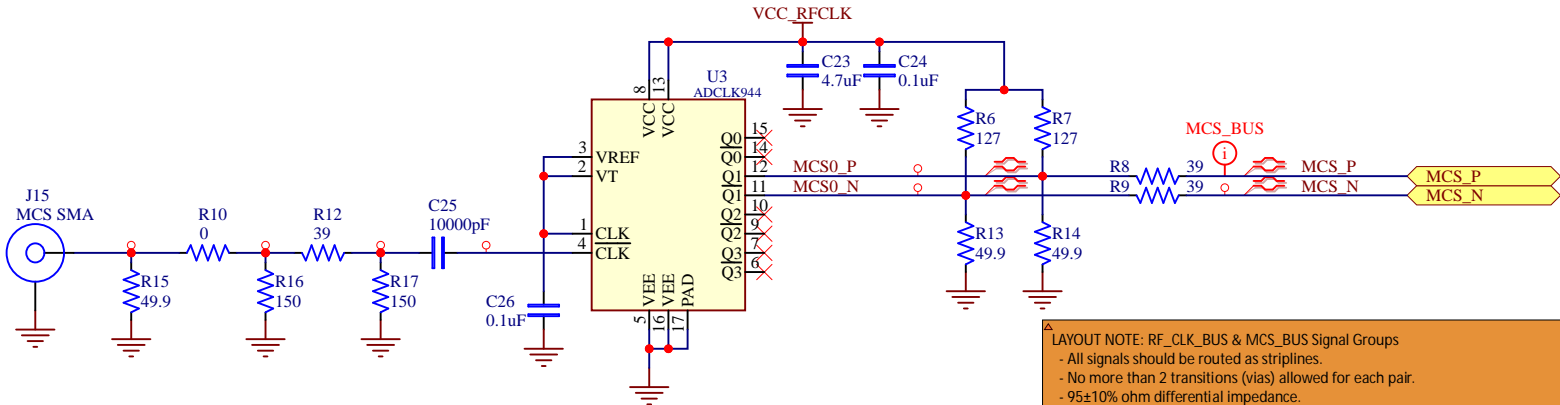
OBSERVATION PORTS



RECEIVE PORTS



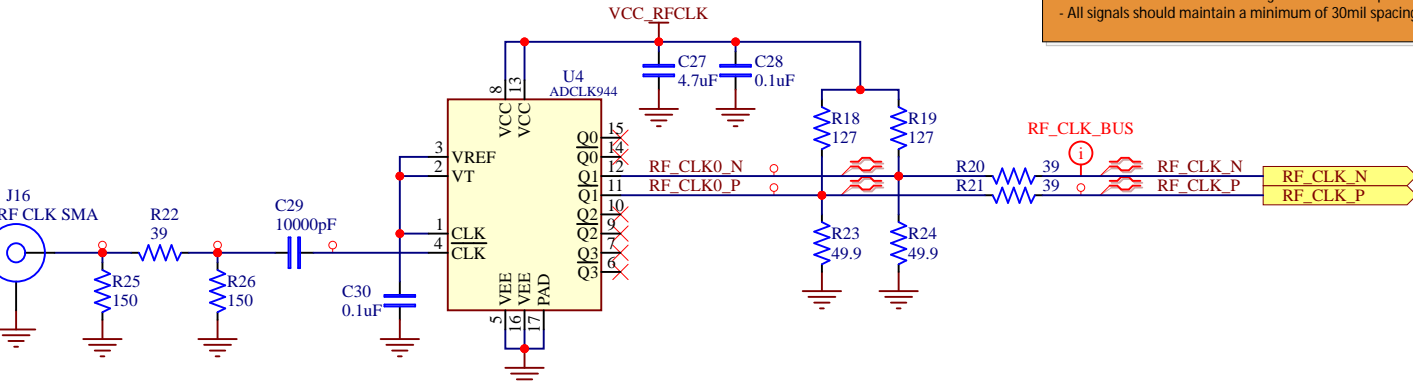
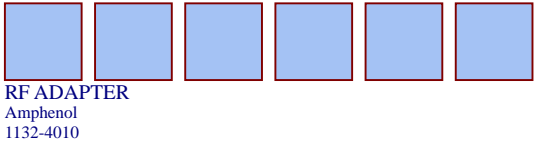
RF DEVICE CLOCK & MCS



LAYOUT NOTE: RF_CLK_BUS & MCS_BUS Signal Groups

- All signals should be routed as striplines.
- No more than 2 transitions (vias) allowed for each pair.
- 95±10% ohm differential impedance.
- The maximum skew between a given differential pair must be less than 1ps.
- All signals should maintain a minimum of 30mil spacing to other signals.

To connect SMPM RF connectors to BytePipe_x9002 SOM using the 1132-4010 Amphenol® RF blind adapter.

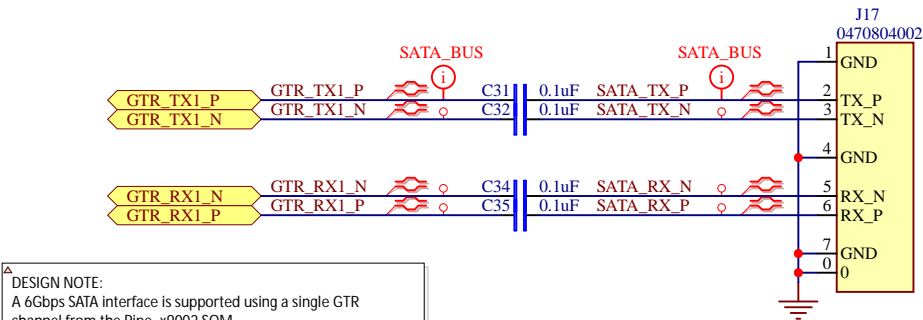


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SYSTEM ENGINEER:	LUKE THOLEN
DATE:	10/11/2021

		NextGen RF Design 2130 Howard Dr W North Mankato, MN 56003	
CUSTOMER: NGRF		PROJECT: BytePipe X9002_HDK	
PAGE TITLE: RF Frontend			
SIZE B	VARIANT: [No Variations]	SHEET 3 OF 7	REV: 2

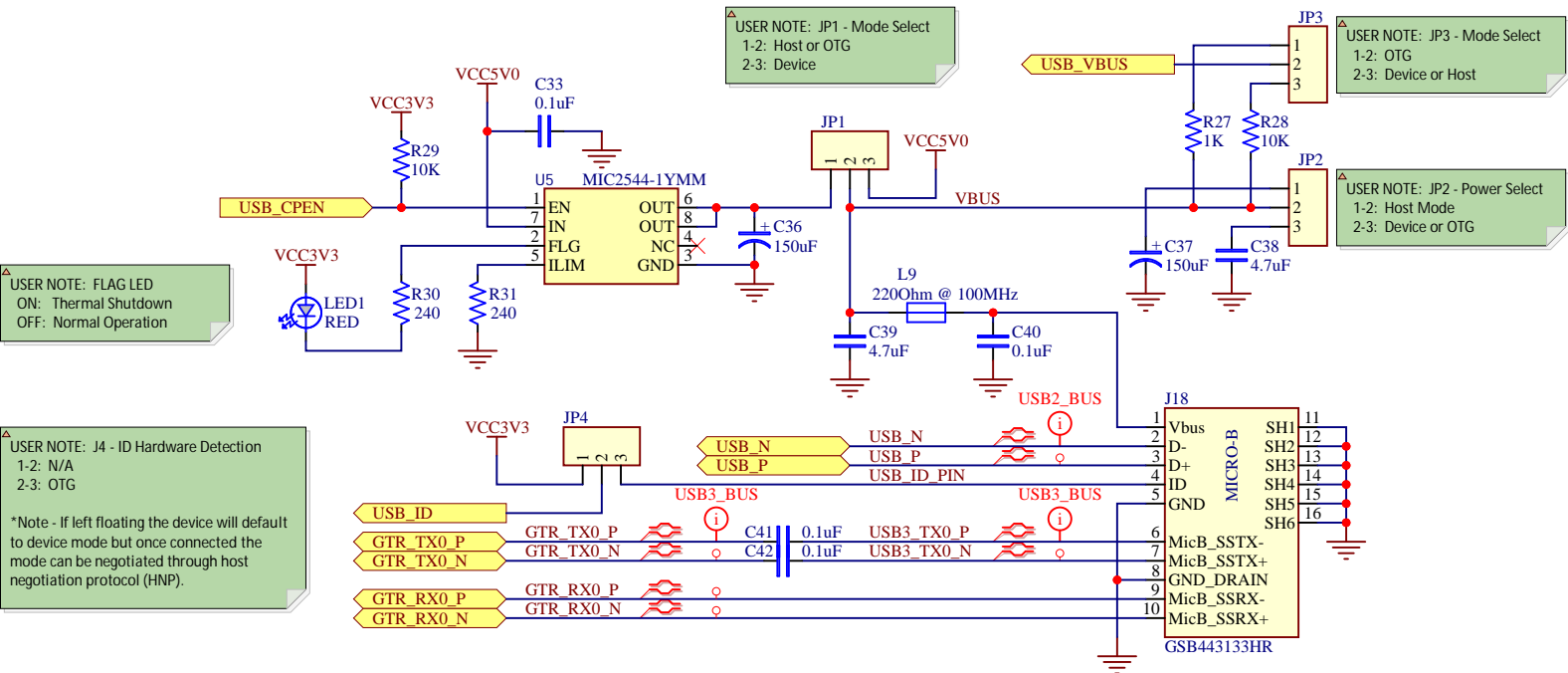
SATA INTERFACE



DESIGN NOTE:
A 6Gbps SATA interface is supported using a single GTR channel from the Pipe_x9002 SOM.

LAYOUT NOTE: SATA_BUS Signal Group
- All signals should be routed as striplines.
- No more than 2 transitions (vias) allowed for each pair.
- 95±10% ohm differential impedance.
- The maximum skew between a given differential pair must be less than 1ps.
- All signals should maintain a minimum of 30mil spacing to other signals.

USB 2.0/3.0 HOST/DEVICE/OTG

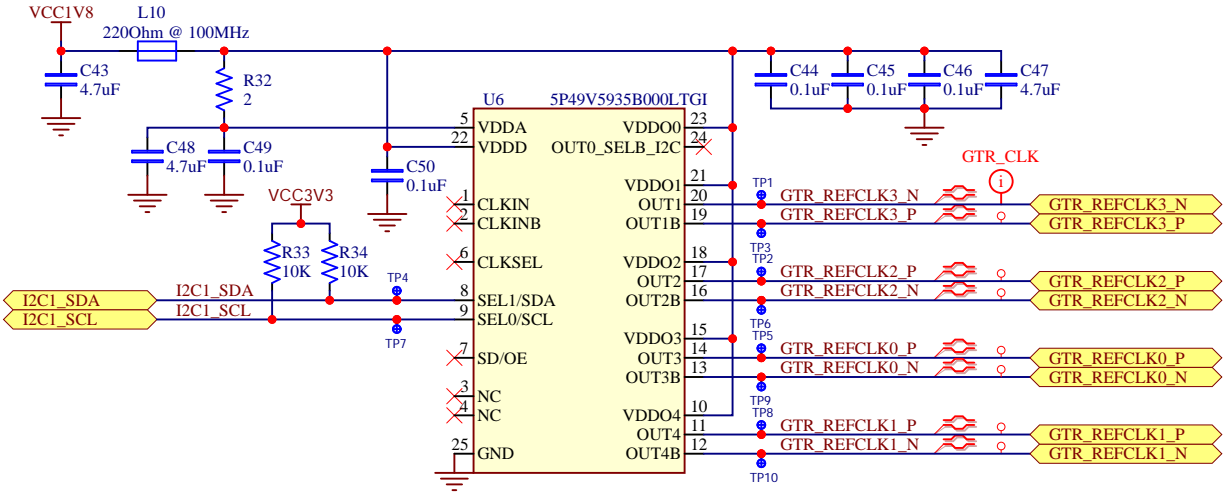


USER NOTE: FLAG LED
ON: Thermal Shutdown
OFF: Normal Operation

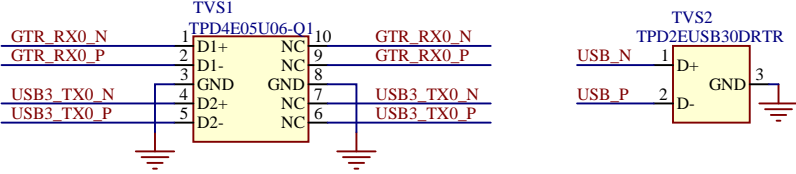
USER NOTE: J4 - ID Hardware Detection
1-2: N/A
2-3: OTG

*Note - If left floating the device will default to device mode but once connected the mode can be negotiated through host negotiation protocol (HNP).

GTR CLOCKS



LAYOUT NOTE: GTR_CLK Signal Group
- All signals should be routed as striplines.
- No more than 2 transitions (vias) allowed for each pair.
- 95±10% ohm differential impedance.
- The maximum skew between a given differential pair must be less than 1ps.
- All signals should maintain a minimum of 30mil spacing to other signals.



LAYOUT NOTE: USB3_BUS & USB2_BUS
- All signals should be routed as striplines.
- No more than 2 transitions (vias) allowed for each pair.
- 95±10% ohm differential impedance.
- The maximum skew within a given differential pair must be less than 0.5ps for USB3_BUS and 5ps for USB2_BUS.
- No skew requirement between TX and RX.
- All signals should maintain a minimum of 30mil spacing to other signals.

DESIGN NOTE:
USB2 is implemented using the dedicated USB2.0 ULP PHY on the BytePipe_x9002 SOM. USB3.0 is implemented using one of four GTR channels.

This hardware supports host, device, or OTG modes depending on the jumper configuration. In host or OTG mode VBUS is supplied from VCC5V0 depending on USB_CPEN state. Supply current limit set to 950mA. In host mode additional capacitance is required.

The following USB modes are supported:

Standard	Mode	Speed
USB2.0	Full Speed	12Mbps
USB2.0	High Speed	480Mbps
USB3.0	Super Speed	5Gbps

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SYSTEM ENGINEER: LUKE THOLEN

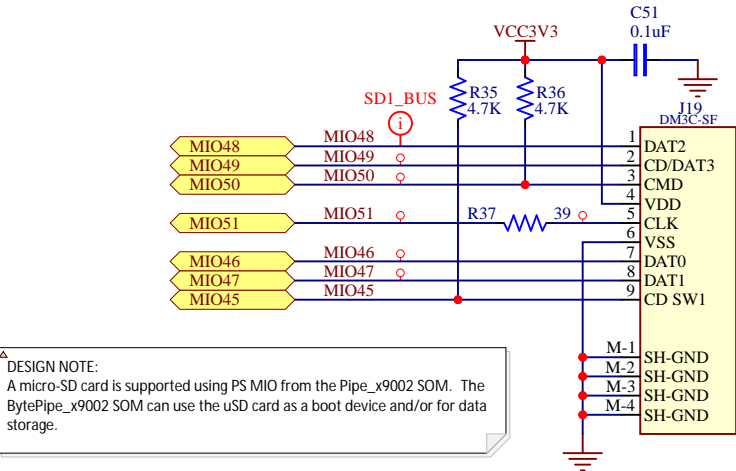
DATE: 10/11/2021

NextGen RF Design
2130 Howard Dr W
North Mankato, MN 56003

CUSTOMER: NGRF
PROJECT: BytePipe X9002_HDK
PAGE TITLE: USB & SATA

SIZE B	VARIANT: [No Variations]	SHEET 4 OF 7	REV: 2
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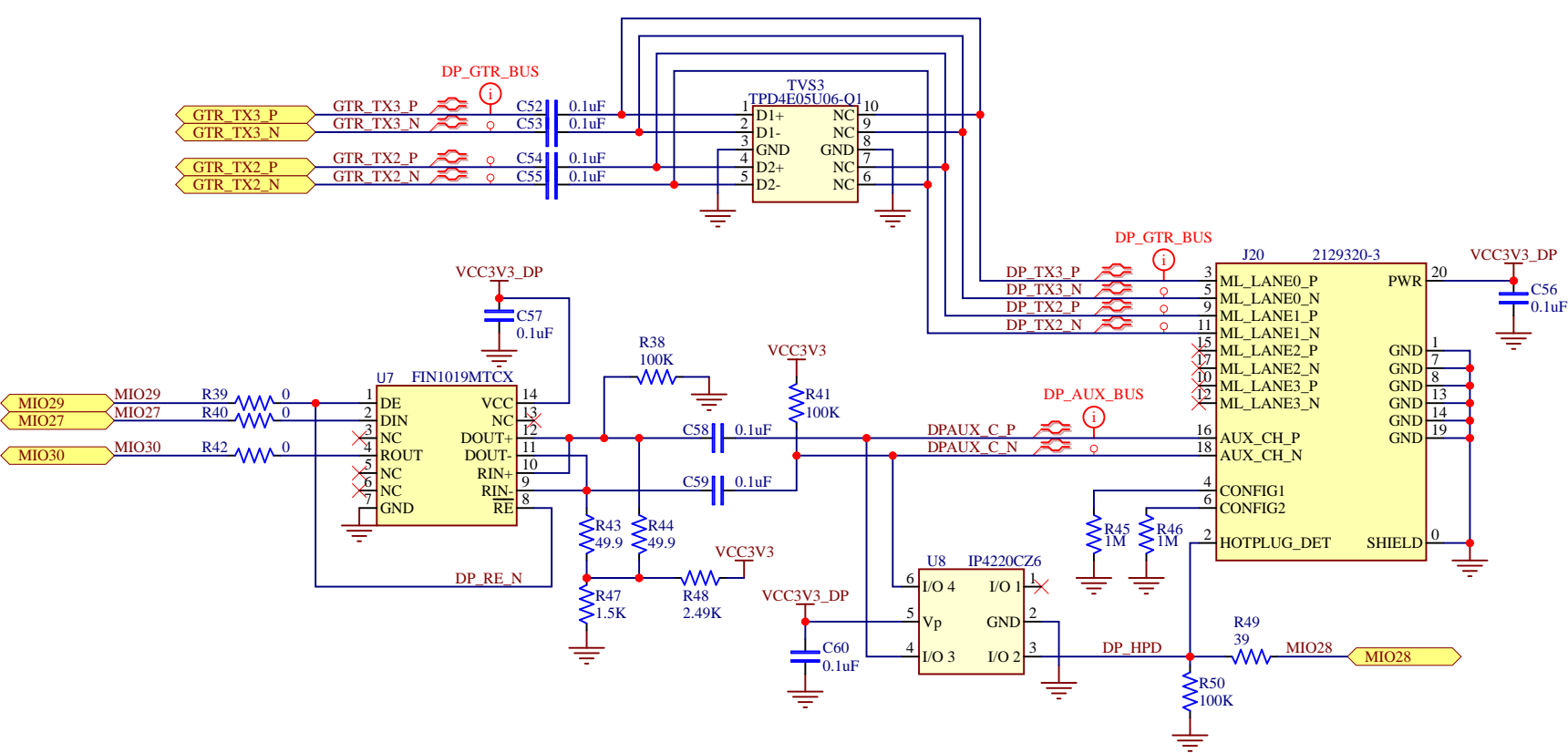
SD CARD



DESIGN NOTE:
A micro-SD card is supported using PS MIO from the Pipe_x9002 SOM. The BytePipe_x9002 SOM can use the uSD card as a boot device and/or for data storage.

LAYOUT NOTE: SD1_BUS Signal Group
- The maximum skew from any signals within the SD_BUS group to the SD1_CLK must be less than 50ps.
- All signals should maintain a minimum of 30mil spacing to other signals.
- Place series resistor of SD1_CLK within 100mils of the SD connector.
- MIO51 is SD1_CLK.

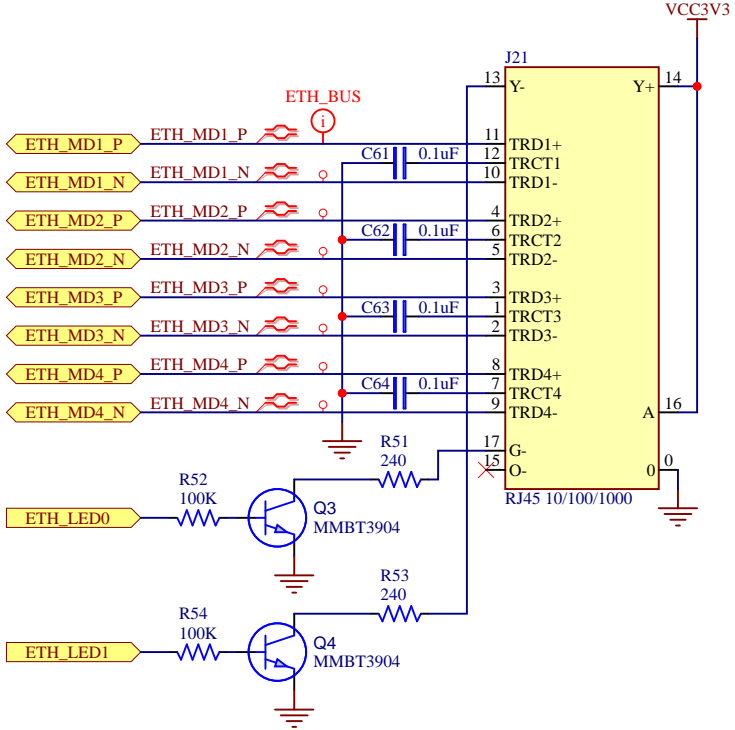
DISPLAY PORT



LAYOUT NOTE: DP_GTR_BUS Signal Group
- All signals should be routed as striplines
- No more than 2 transitions (vias) allowed for each pair
- 95±10% ohm differential impedance
- 4x spacing between pairs
- The maximum skew within a given differential pair must be less than 1.0ps.
- The maximum skew between the slowest differential pair (mid-point) and the fastest differential pair must be less than 20ps.
- All signals should maintain a minimum spacing to other signals within the same group of 8mils and 30 mils to other groups.
- All signals within the group should be routed on the same layer.

LAYOUT NOTE: DP_AUX_BUS Signal Group
- All signals should be routed as striplines
- No more than 2 transitions (vias) allowed for each pair
- 95±10% ohm differential impedance
- 4x spacing between pairs
- The maximum skew within a given differential pair must be less than 1.0ps.

10/100/1000 ETHERNET



USER NOTE: Ethernet LEDs
GREEN : Speed
YELLOW: Activity

LAYOUT NOTE: ETH_BUS Signal Group
- All signals should be routed as striplines.
- No more than 2 transitions (vias) allowed for each pair.
- 95±10% ohm differential impedance.
- The maximum skew between a given differential pair must be less than 2ps.
- The group as a whole should maintain a minimum of 30mil spacing to other signals outside the group.
- The maximum skew between the slowest differential pair (mid-point) and the fastest differential pair of the signal group must be less than 10ps.

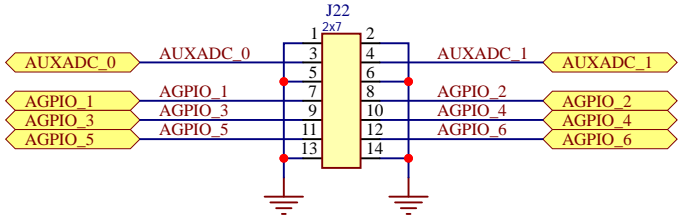
DESIGN NOTE:
A Display Port output is supported using PS MIO and dual GTR channels from the Pipe_x9002 SOM. The PS MIO supports the display port auxiliary channel. A display port auxiliary generator is used to convert the single ended uni-directional PS MIO signals to a differential bi-directional display port channel. GTR channels two and three are used for high speed video data.

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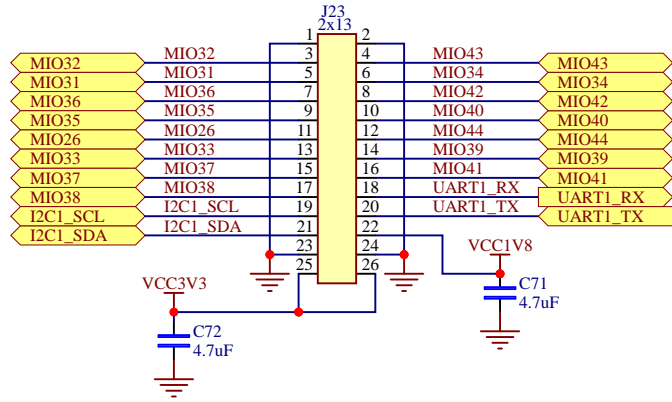
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SYSTEM ENGINEER:	LUKE THOLEN
DATE:	10/11/2021

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CUSTOMER:		NGRF	
PROJECT:		BytePipe X9002_HDK	
PAGE TITLE:		DisplayPort & Ethernet	
SIZE	VARIANT:	SHEET	REV:
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RFIC GPIO



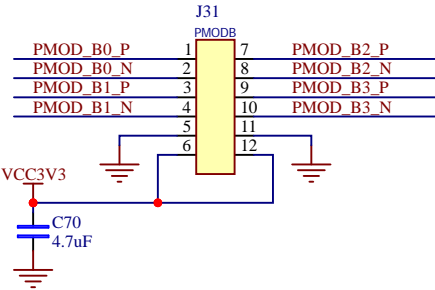
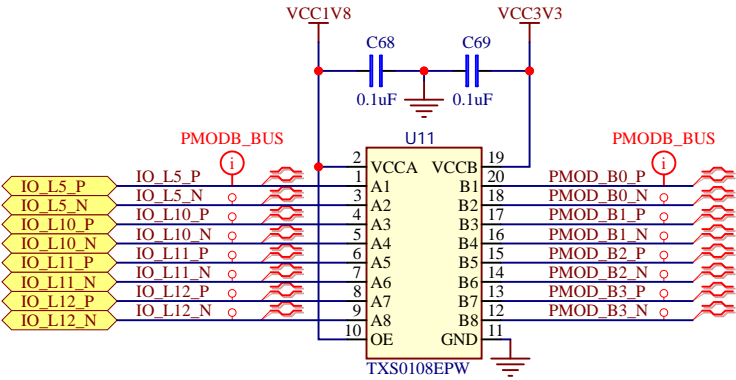
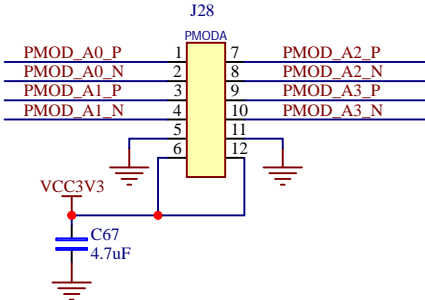
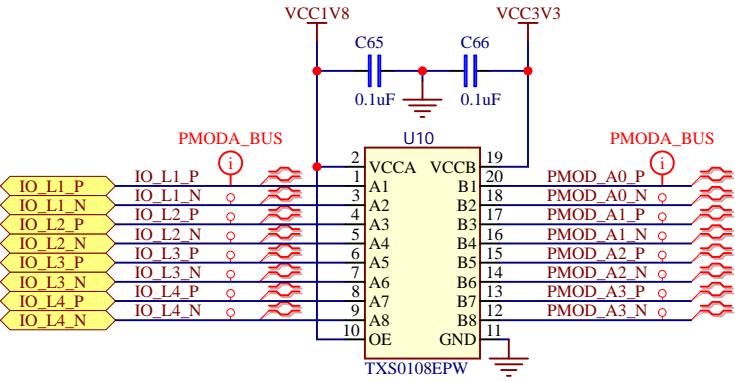
PS MIO



BANK 501 Peripherals																										
MIO	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51
SD1																										
CAN0																										
CAN1																										
SPI0																										
SP1																										
I2C0																										
DP																										
GEM0																										
GEM1																										

Bank 501 can be configured as GPIO or as a variety of peripherals. This bank supports 1.8V, 2.5V, or 3.3V supplied by the host. Peripherals can also be routed through programmable logic and connected to host using programmable logic pins. The display port requires one or two transmit channels

PL PMODs



LAYOUT NOTE: PMODA_BUS & PMODB_BUS Signal Groups

- All signals should be routed as striplines.
- No more than 2 transitions (vias) allowed for each pair.
- 95±10% ohm differential impedance.
- The maximum skew between a given differential pair must be less than 2ps.
- The maximum skew between the slowest pair and fastest pair within a group must be less than 10ps.
- Signals within the same group should be routed together as a bus.
- All signals should maintain a minimum of 30mil spacing to other signals outside the bus.

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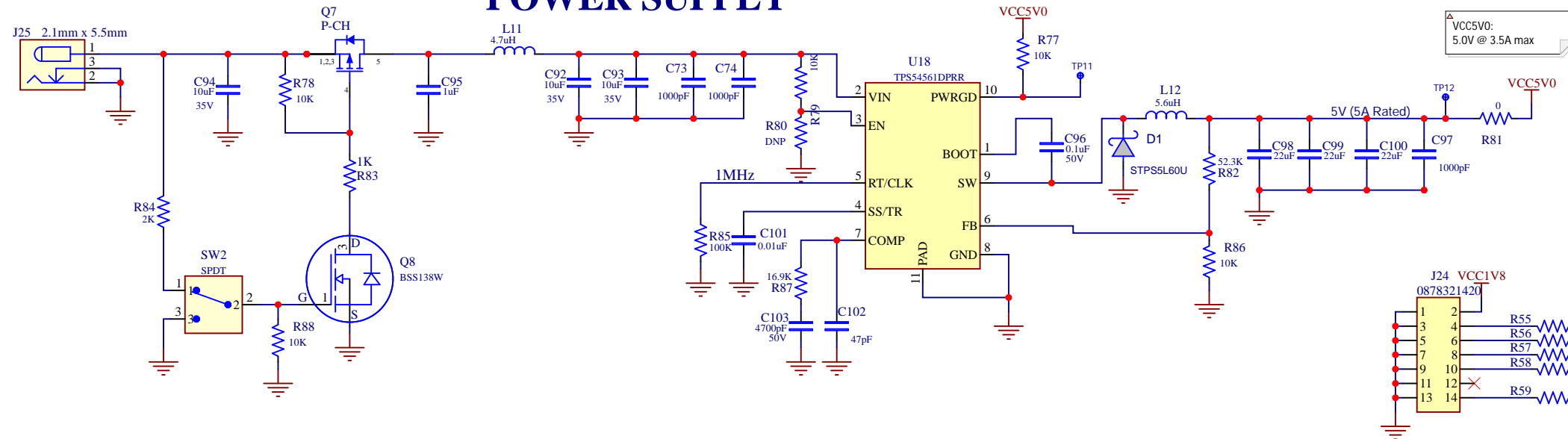


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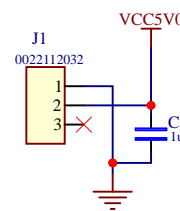
CUSTOMER: NGRF
PROJECT: BytePipe X9002_HDK
PAGE TITLE: User I/O

SIZE	VARIANT:	SHEET	REV:
B	[No Variations]	6 OF 7	2

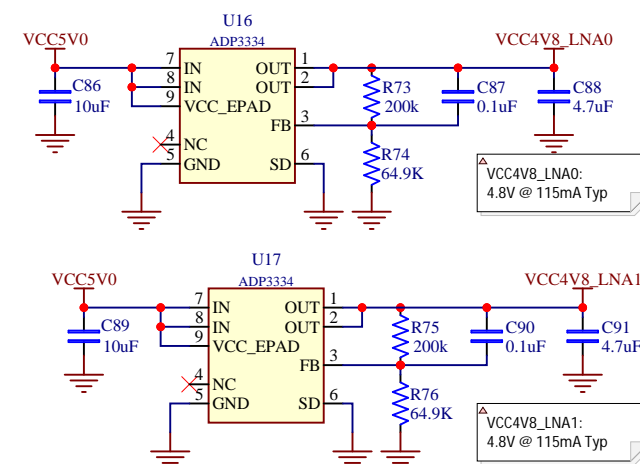
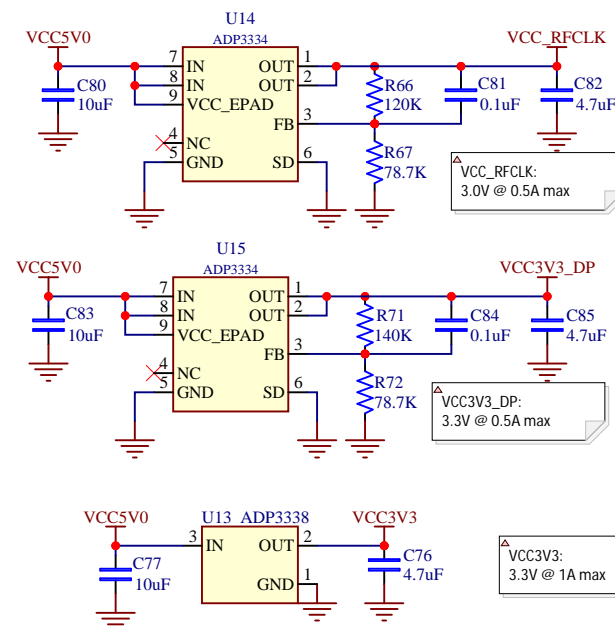
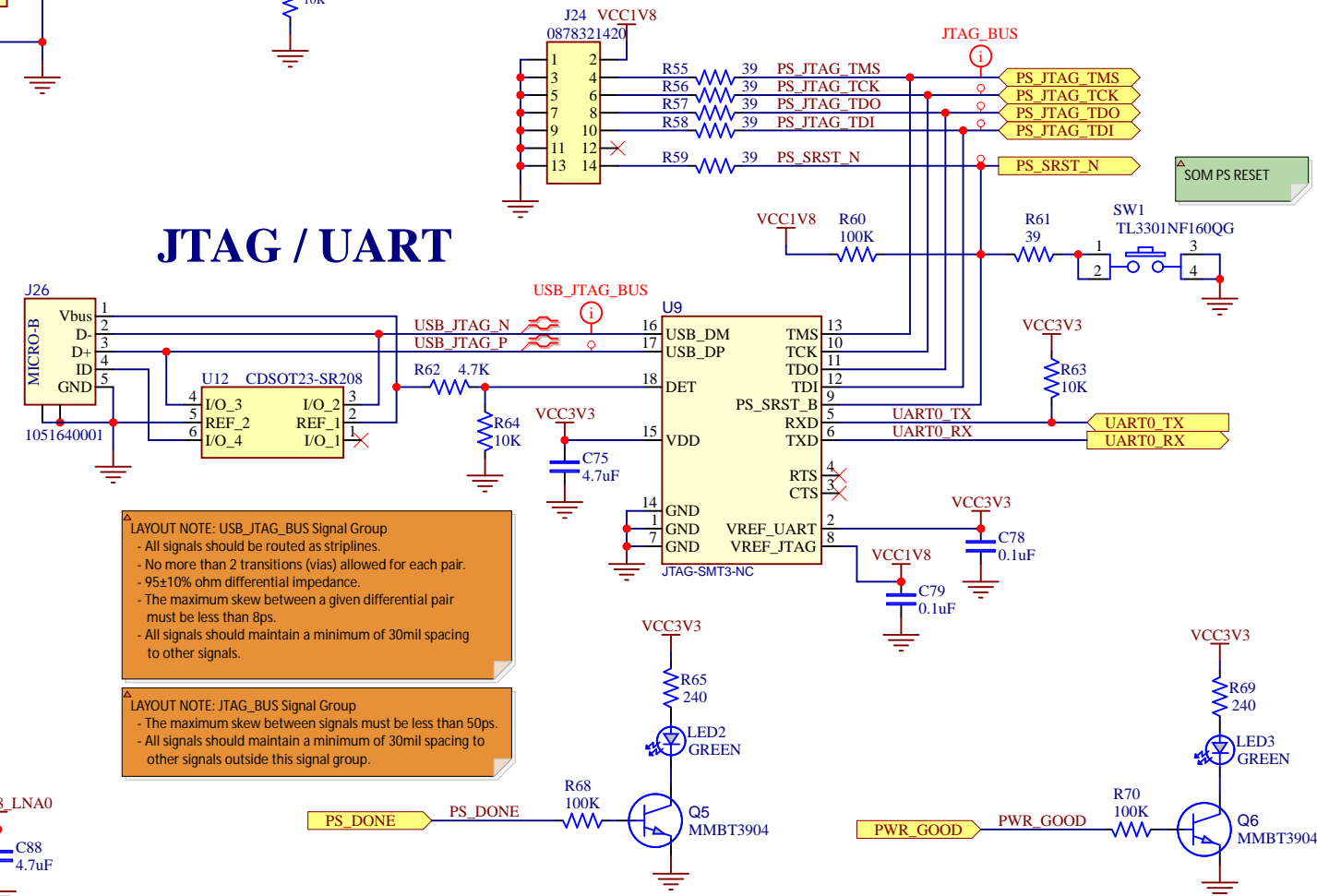
POWER SUPPLY



Keyed Fan Header



JTAG / UART



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CUSTOMER:	NGRF
PROJECT:	BytePipe X9002_HDK
PAGE TITLE:	JTAG & Power

	SIZE
	B

VARIANT:
[No Variations]

SHEET

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REV: 2